Electronic Version
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Claims

[c1] 1. A display controller for producing a multi-gradation image on a display device formed by a plurality of binary-state pixels in an array through a plurality of consecutive frames, the plurality of binary-state pixels being classified into a plurality of pixel groups having an identical size, the display controller comprising:
column addressing means for designating a column number of a desired pixel;
row addressing means for designating a row number of the desired pixel;
an image memory for providing gradation data in response to the column and row numbers of the desired pixel, the gradation data being indicative of a gradation level to be produced at the desired pixel;
a waveform pattern memory for providing the display device with plural sets of waveform pattern signals, each set having an identical number of waveform pattern signals, each waveform pattern signal having a predetermined number of bits and producing a different gradation level when applied to a pixel, each bit being provided for displaying during a corresponding frame of the plurality of consecutive frames; and

a waveform pattern selector for outputting a waveform pattern selecting signal in response to the column and row numbers of the desired pixel such that the waveform pattern memory provides two adjacent pixel groups with two different sets of the plural sets of waveform pattern signals, respectively, wherein:

the waveform pattern memory determines a selected set of the plural sets of waveform pattern signals in response to the waveform pattern selecting signal, determines a selected waveform pattern signal of the selected set of waveform pattern signals in response to the gradation data, and provides the bits of the selected waveform pattern signal, one bit per frame, over the plurality of consecutive frames;

the two different sets of the plural sets of waveform pattern signals provided for the two adjacent pixel groups, respectively, are so designed as to operate the two adjacent pixel groups at two different states during at least one frame of the plurality of consecutive frames; and

the plurality of consecutive frames is displayed at a frame rate high enough for preventing visual disturbances.

[c2] 2. The display controller according to claim 1, wherein:

the frame rate is equal to or higher than 120 Hz.

[c3] 3. The display controller according to claim 1, wherein: the frame rate is equal to or higher than (2^n x 15) Hz where n is equal to or larger than 3.

[c4] 4. The display controller according to claim 1, wherein: the waveform pattern memory is restricted to provide only two sets of waveform pattern signals.

[c5] 5. The display controller according to claim 4, wherein: the waveform pattern memory stores a first set of the two sets of waveform pattern signals and derives a second set of the two sets of waveform pattern signals from the first set of the two sets of waveform pattern signals by using the waveform pattern selecting signal.

[c6] 6. The display controller according to claim 4, wherein: the waveform pattern selecting signal is a binary selecting signal, which is restricted to select between the two sets of waveform pattern signals.

[c7] 7.The display controller according to claim 4, wherein: the multi-gradation image has 2^m gradations and is produced through consecutive 2^n frames where m is equal to or smaller than n and n is equal to or larger than 3, and

each set of the two sets of waveform pattern signals has 2^m waveform pattern signals for producing the 2^m gra-

dations, respectively, each waveform pattern signal having 2^n bits.

[c8] 8.The display controller according to claim 7, wherein: the frame rate is equal to or higher than (2^n x 15) Hz.

[c9] 9.The display controller according to claim 1, wherein: the waveform pattern selector outputs the waveform pattern selecting signal in response to a least significant bit of the column number and a least significant bit of the row number.

[c10] 10.The display controller according to claim 9, wherein: the waveform pattern selector is implemented by an Exclusive-OR logical circuit such that the waveform pattern selecting signal is a result of an Exclusive-OR logical operation between the least significant bit of the column number and the least significant bit of the row number.

[c11] 11.The display controller according to claim 1, wherein: each of the plurality of pixel groups is formed by a single pixel of the plurality of binary-state pixels.

[c12] 12.The display controller according to claim 1, wherein: the display device is a color display device such that each of the plurality of binary-state pixels is constructed to produce one of three primary colors: red, green, and blue, and

each of the plurality of pixel groups is formed by a single pixel of the plurality of binary-state pixels regardless of its color.

[c13] 13.The display controller according to claim 1, wherein:
the display device is a color display device such that every three pixels of the plurality of binary-state pixels makes up a color pixel unit and produces three primary colors: red, green, and blue, respectively, and
each of the plurality of pixel groups is formed by a single one of the color pixel units.

[c14] 14.The display controller according to claim 1, further comprising:
a look-up table coupled between the image memory and the waveform pattern memory for transferring the gradation data provided by the image memory, thereby expanding the number of bits of the gradation data.

[c15] 15.Thedisplay controller according to claim 1, further comprising:
a look-up table coupled between the image memory and the waveform pattern memory for transferring the gradation data provided by the image memory, thereby performing Gamma corrections on the gradation data.

[c16] 16. The display controller according to claim 1, wherein:

the column addressing means is implemented by a pixel counter.

[c17] 17. The display controller according to claim 1, wherein: the row addressing means is implemented by a scan line counter.

[c18] 18.Thedisplay controller according to claim 1, further comprising:
a frame counter for sequentially indicating the waveform pattern memory with each of the plurality of consecutive frames.

[c19] 19.A method of producing a multi-gradation image on a display device formed by a plurality of binary-state pixels in an array through a plurality of consecutive frames, comprising:
defining an elementary 2 x 2 pixel cell on the display device, the elementary 2 x 2 pixel cell having two pixels along a first diagonal and two pixels along a second diagonal;
defining a first set of waveform pattern signals and a second set of waveform pattern signals, each set having an identical number of waveform pattern signals, each waveform pattern signal having a predetermined number of bits and producing a different gradation level when applied to a pixel, each bit being provided for displaying

during a corresponding frame of the plurality of consecutive frames;

providing the two pixels along the first diagonal with the first set of waveform pattern signals and the two pixels along the second diagonal with the second set of waveform pattern signals such that the two pixels along the first diagonal and the two pixels along the second diagonal are operated at different states during at least one frame of the plurality of consecutive frames; and

displaying the plurality of consecutive frames at a frame rate high enough for preventing visual disturbances.

[c20] 20. The method according to claim 19, wherein:

the multi-gradation image has 2^m gradations and is produced through consecutive 2^n frames where m is equal to or smaller than n and n is equal to or larger than 3;

each set of the first and second sets of waveform pattern signals has 2^m waveform pattern signals for producing the 2^m gradations, respectively, each waveform pattern signal having 2^n bits; and

the frame rate is equal to or higher than (2^n x 15) Hz.